

Appl. No. 10/031,332
Amdt. Dated August 19, 2005
Reply to Office action of March 24, 2005
Attorney Docket No. P11107/000500-335
EUS/J/P/05-6146

REMARKS/ARGUMENTS

1.) Claim Amendments

The Applicant has amended Claims 1 – 3 and 6 – 14. Applicant respectfully submits no new matter has been added. The applicant has cancelled claims 4 and 5. Accordingly claims 1- 3 and 6 – 14 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2.) Examiner Objections – Specification

The Examiner objected to the specification because of several informalities. The Applicant thanks the Examiner for his careful review of the specification. In response, the Applicant has modified the specification as suggested by the Examiner. The Examiner's consideration of the amendments to the Specification is respectfully requested.

3.) Claim Rejections – 35 U.S.C. § 112

The Examiner rejected claims 4, 9, and 10 under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention and in particular as to recite limitations having an insufficient antecedent basis. In order to expedite allowance of this application, the Applicant has canceled claims 4 and 5 without prejudice. Therefore, this rejection with respect to these claims is deemed to be moot. The applicant has further amended claim 9 to overcome the examiner's 112 rejection.

4.) Claim Rejections – 35 U.S.C. § 102(b)

The Examiner rejected claims 1 and 2 as being anticipated by Shuler, Jr. (US 4,912,629). The Applicant respectfully traverses the examiner's rejection and has further amended independent claim 1 to more clearly and distinctly define the subject matter, which the Applicant regards as his invention. A favorable reconsideration is respectfully requested.

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The present invention discloses and claims a processor architecture adapted to program languages operating with a sequential flow of instructions and handling data through the use of simple values and lists and dynamically allocated arrays. The processor architecture comprises instruction holding means, data memory means storing data objects, and execution means. The processor architecture further comprises means for storing and handling function-argument-values further comprising simple values and references to data objects in dependence of an actual instruction from the instruction holding means. The Applicant submits that such dependence is called a "binding" in accordance with the teachings of the present invention. The means for storing and handling function-argument-values is further suitable for substituting a function parameter in an actual instruction with an actual function argument value and for providing the actual instruction and the actual function argument value to the execution means. In accordance with the present invention, the means for storing and handling function argument values is further separate from the execution means and from the instruction holding means. The processor architecture according to the present invention further comprises means to increment reference counts to a data object and to decrement reference counts to a data object in dependence of an actual instruction from the instruction holding means, and to store a reference to the data object in dependence of the means, which handles simple values and references.

The Applicant respectfully submits that such processor architecture comprising means for storing and handling function-argument-values and providing a "binding" to an actual instruction from instruction holding means and for providing the actual instruction and an actual function-argument-value to an execution means is neither disclosed nor taught by Shuler. The Shuler reference furthermore fails to disclose or teach such means for storing and handling function-argument-values being separate from the execution means. In that regard, the Shuler reference merely discloses a processing system comprising a list processor for handling data objects organized in lists and a garbage manager operating according to a predefined processing sequence

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for cleaning up references to objects that have become dispensable. The garbage manager in figure 4 executes commands in respect to the reorganization of a linked list and exchanges command information on one interface with the list processor and data objects on a second interface with the list processor.

According to Shuler, the processing steps performed by the garbage manager follow a fixed succession of predefined instructions instead of being adaptable to current instructions from instruction holding means. Accordingly, the Applicant respectfully submits that the Shuler reference neither shows nor suggests instruction-holding means holding instructions to be executed by processing means as recited by the currently pending claims.

Moreover, the function codes referred to in the Shuler reference refer to the storage and retrieval operation on a memory manager performed along with address information used within the memory manager. However nothing in the Shuler reference discloses or teaches the means for storing and handling function-argument-values and the means providing a binding of function-argument-values and actual instructions.

Furthermore, nothing in the Shuler reference discloses or teaches separating the execution means providing an actual instruction and an actual function-argument-value from the means for handling a binding of the function-argument-value and the actual instruction.

The Applicant therefore submits that independent Claim 1 is patentable over the cited references. As for the dependent claim 2, this dependent claim recites further limitations in combination with the novel elements of claim 1. Therefore, the Applicant respectfully requests the allowance of claims 1 and 2.

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5.) Claim Rejections – 35 U.S.C. § 103 (a)

The Examiner rejected claims 3 – 10 and 12 – 14 under 35 U.S.C. § 103(a) as being unpatentable over Shuler, Jr. (US 4,912,629) in view of Zee (US 4,530,049). In order to expedite allowance of this application, the Applicant has canceled the claim 4 without prejudice. Therefore, this rejection with respect to this claim is deemed to be moot.

With regard to the Zee reference, the Zee reference discloses a processing system comprising an instruction stack storing instructions associated with respective function argument values. Accordingly, the applicant respectfully submits that the Zee reference also fails to show or suggest a processor architecture comprising separate means for storing instructions and for binding the function argument values to an actual instruction from the instruction holding means.

Furthermore, dependent claims 3, 5– 10 and 12 – 14 recite further limitations in combination with the novel and non-obvious subject matter of claim 1. The applicant therefore respectfully requests the allowance of claims 3, 5– 10 and 12 – 14.

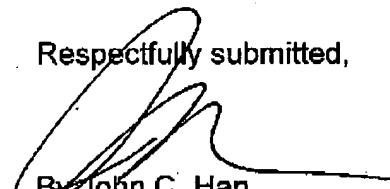
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CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,



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